SR250

Технические характеристики

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Gated Integrators and Boxcar Averagers

SR250 — Gated integrator with gate width to 2 ns

- Gate width from 2 ns to 15 µs (expandable to 150 µs)
- Internal rate generator
- Active baseline subtraction
- Shot-by-shot output
- Gate output for precise gate timing
- Average 1 to 10,000 samples
- DC to 20 kHz repetition rate
- Low jitter (<20 ps + 0.01 % of delay)

SR250 Gated Integrator

The SR250 Gated Integrator is a versatile, high-speed NIM module designed to recover fast analog signals from noisy backgrounds.

The SR250 consists of a gate generator, a fast gated integrator, and exponential averaging circuitry. The gate generator, triggered internally or externally, provides an adjustable delay from a few nanoseconds to 100 ms before it generates a continuously adjustable gate with a width between 2 ns and 15 µs. The gate delay can be set from the front panel or automatically scanned by applying a rear-panel control voltage. Scanning the gate allows the recovery of entire waveforms.

The fast gated integrator integrates the input signal during the gate. The output from the integrator is then normalized by the gate width to provide a voltage proportional to the average of the input signal during the sampling gate. This signal is further amplified and sampled by a low-droop sample-and-hold amplifier, and output via a front-panel BNC connector. The last sample output provides a shot-by-shot analysis of the signal, and makes the instrument a particularly useful component in a computer data acquisition system.

Triggering

The SR250 may be triggered internally or externally. The internal rate generator is continuously variable from 0.5 Hz to 20 kHz in nine ranges. The external trigger pulse may be as short as 5 ns, allowing the unit to be triggered with fast pulses from photodiodes and photomultipliers. Single shot and line triggering can also be selected.

Signal Inputs

The sensitivity (Vin/Vout) of the instrument may be set from 1 V/V to 5 mV/V. If additional gain is required, the SR250 can be used with the SR240A preamplifier. The input is protected to 100 V and has a 1 MΩ input impedance. An input filter rejects unwanted signals before the input is sampled by the integrator. Unwanted DC input offsets are easily nulled with a 10-turn potentiometer.

Gate Timing

The delay of the sample gate from the trigger is set by the delay multiplier and scale. The delay scale is multiplied by the setting on the 10-turn multiplier dial, allowing continuously adjustable delays from a few nanoseconds to 100 ms. The delay multiplier may also be changed from the rear-panel control voltage input—a useful feature in applications requiring a scanning gate. Zero to ten volts at this input overrides the front-panel 0 to 10× delay multiplier. Insertion delay from trigger to gate is only 25 ns, and gate-delay jitter is only 20 ps + 0.01 % of the full-scale delay.

The width of the sampling gate may be continuously adjusted from 2 ns to 15 µs over eight width ranges. A simple modification of the unit allows gate widths of up to 150 µs. The front-panel gate output provides a representation of the gate that can be overlayed with the signal on an oscilloscope to provide a precise display of the gate timing.

Signal Outputs

A moving exponential average of 1 to 10,000 samples can be selected from the front panel. This traditional averaging technique is useful for pulling small signals from noisy backgrounds. In the case of a random white noise background, the signal-to-noise ratio increases by the square root of the number of samples in the average. This allows a S/N improvement of up to a factor of 100 using this technique alone. If no averaging is desired, or if averaging is to be performed on a computer, the last sample output provides a voltage proportional to the average value of the input signal during the last gate period.

Average Reset

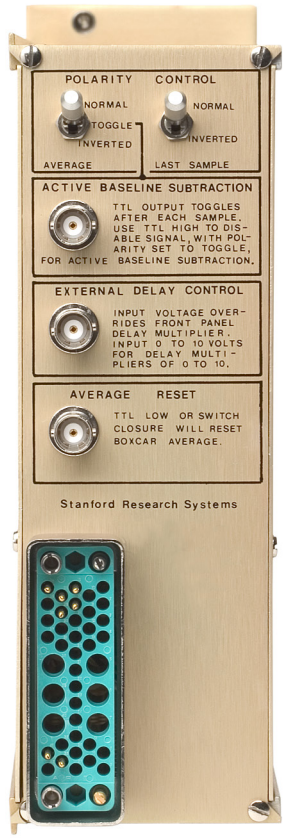
The reset button sets the average output to zero. The average may also be reset by a rear-panel logic input. The average reset input will accept a TTL signal or a switch closure to ground to reset the moving average output.

Polarity Control and Active Baseline Subtraction

The polarity of the last sample and averaged outputs is controlled by rear-panel toggle switches. Positive outputs can be selected for negative signals, and vice versa, allowing easy interfacing with unipolar analog-to-digital conversion systems. In addition to the traditional averaging modes, the SR250 possesses a unique Active Baseline Subtraction mode which allows you to actively cancel baseline drift. In the Active Baseline Subtraction mode, the SR250 is triggered at twice the source repetition rate. On alternate triggers (when the signal is not present) only the baseline is sampled, and the SR250 inverts the polarity of the last sample output before it is added to the moving average. Thus, any baseline drift not associated with the source will be subtracted out.

Additional Outputs

The signal input is passed on to the signal output by a length of coaxial cable for termination and for gate timing. It is delayed exactly 3.5 ns from the input, and can be terminated to optimize either signal gain or response time. The gate output provides a pulse synchronized with the internal gate signal. The gate output is timed so that it can be overlayed with the signal output for precise adjustment of gate timing. The busy output provides a TTL timing pulse which is high while the unit is integrating, and goes low when the SR250 is ready to accept another trigger. These outputs help simplify experimental setup and troubleshooting.



SR250 rear panel

Ordering Information

SR250	Gated integrator

Trigger

Internal trigger	0.5 Hz to 20 kHz
Line trigger	The gate generator may be triggered from AC line with adjustable phase.
External trigger	1 MΩ input impedance. Trigger threshold adjustable from 0.5 to 2 V. Input protected to ±100 VDC. Trigger pulse must be over threshold for >5 ns with a rise time <1 µs.
Manual trigger	The unit will trigger if trigger threshold is scanned through 0 VDC.
Trigger LED	LED blinks with each trigger.

Delay

Delay scale	1 ns to 10 ms
Delay multiplier	0 to 10× using 10-turn dial
Insertion delay	25 ns
Accuracy	2 ns or 5 % of full-scale delay, whichever is larger
Jitter	<20 ps or 0.01 % of full-scale delay, whichever is larger
Ext. delay control	Rear-panel 0 to 10 VDC input overrides front-panel delay multiplier. Used by SR200 / SR245 to scan gate.

Gate Width

Width scale	1, 3, 10, 30, 100, 300 ns, 1, 3 µs
Width multiplier	Adjustable from 1× to 5×
Width accuracy	2 ns or 20 % of full scale, whichever is greater
Minimum width	2 ns, FWHM

Signal

Sensitivity (V_{in}/V_{out})	1 V/V to 5 mV/V in a 1-2-5 seq.
Accuracy	3 % for gate widths >10 ns, decreasing to 50 % for a 2 ns gate
Filter	DC coupled, or AC coupled above 10 Hz or 10 kHz
Offset control	±0.4 VDC using 10-turn dial
Over range LED	Indicates input is >2 VDC or LAST SAMPLE is greater than 10 VDC

Last Sample

Output	±10 VDC, 10 mA (20 mA short circuit limit), impedance <1 Ω
Polarity switch	Inverts LAST SAMPLE output
Responsivity	95 % (no more than 5 % of the previous last sample remains)

Averaging

Type	Exponential moving average
Number of samples	1, 3, 10, 30, ... to 10,000 LAST is selected for no averaging
Average output	±10 VDC full scale, 10 mA (20 mA short circuit limit). Impedance <1 Ω
Droop rate	When no ext. triggers are present, droop rate is <1 % per minute (1 to 30 samples), and <0.01 % per minute (100 to 10,000 samples).
Average polarity and baseline subtraction	Rear-panel switch sets polarity of LAST SAMPLE before it is added to the average. Can also be used to invert polarity of average output. In TOGGLE position, every other sample is subtracted from the average. By triggering at twice the experiment's rep rate, baseline will be sampled on alternate triggers and subtracted from the average.
Toggle output	Rear-panel TTL signal changes state with each trigger. Output used with Active Baseline Subtraction feature to indicate if next sample will be added to, or subtracted from, the moving average. Toggle output can drive 50 Ω loads to +2 VDC.
Reset button	Resets average to zero
Remote reset	Rear-panel input resets average with a TTL low or switch closure.

Signal Input and Output

Signal input	1 MΩ input impedance, ±2 VDC usable range, protected to 100 VDC. Input offset drift <0.5 mV/hr. after 20 min. warm-up. Shot noise at input <0.5 mV. Coherent pickup <5 mV (easily cancelled with offset knob in fixed gate applications).
Signal output	SIGNAL OUTPUT is the input signal delayed by 3.5 ns. (Used to terminate input signal and to time gate with respect to signal output.)

Gate and Busy Outputs

Gate output	200 mV pulse marks exact position of gate with respect to signal output. ±1 ns accuracy (50 Ω load)
Busy output	TTL signal indicates output data is ready. High from trigger signal until unit is ready for next trigger (45 µs min., longer for long delays or gate widths). Drives 50 Ω load to 2 VDC.

General

Power supplies	+24 V/135 mA, +12 V/380 mA, –12 V/230 mA, –24 V/150 mA. 14 W. Power from a standard NIM crate (SR280).
Mechanical	Dual-width NIM enclosure
Dimensions	2.7" × 8.174" × 11.5" (WHD)
Warranty	One year parts and labor on defects in materials and workmanship

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